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~~A~~ METHOD AND APPARATUS FOR CONTROLLING ~~THE~~ HEAD VELOCITY IN~~OF~~ A DISK ~~HARD~~ DRIVE DURING RAMP LOAD/UNLOAD

FIELD OF THE INVENTION

The present invention relates to ~~a method and apparatus for~~ controlling ~~the transducer~~ head velocity in~~of~~ a disk drive during ~~a~~ ramp load or unload ~~procedure~~.

~~More particularly, the present invention provides for the control of the transducer heads using a microprocessor to determine the speed of the heads and, accordingly, to make velocity adjustments.~~

BACKGROUND OF THE INVENTION

D~~A hard~~ disk drives include ~~is a device with~~ one or more disks~~, or platters,~~ on which digital information is stored as~~in the form of~~ magnetic charges. The disk (or disks) is ~~are~~ mounted on ~~and rotated by~~ a ~~cylindrical~~ spindle rotated by a spindle motor ~~assembly~~. An actuator assembly includes an actuator arm and ~~Contemporary hard disk drives typically include an actuator, a rotary actuator structure that is powered by~~ a voice coil motor ("VCM"). The ~~, an~~ actuator arm extends~~ing~~ from the VCM and supports a slider that includes a read/write head. The head reads from and writes to the disk as the slider flies over the disk on an air cushion. T~~,~~he VCM positions the head ~~and a transducer head disposed at the end of the actuator arm. The rotary actuator structure positions one or more slider head assemblies~~ at desired locations relative to the ~~surfaces of the magnetic disk or~~ disks~~. A hard disk read/write head, which is used to read and~~

~~write the data to and from the magnetic disk, is mounted onto the slider head assembly. Thus, the slider physically supports the head and holds it in the correct position relative to the hard disk platter as the head floats over the surface. While the actuator assembly is actuated by a VCM, a spindle motor rotates the magnetic disk or disks.~~

D~~In modern d~~isk drives have been designed ~~the heads~~ with a landing zone ~~are generally parked, or stopped,~~ at the inner diameter of the disk to park the head. The ~~, such as a landing zone, whenever the spindle assembly is at rest. A~~ landing zone is ~~an area of the disk that is designated as either~~ a takeoff or landing spot for the heads as~~while~~ the disk~~spindle~~ starts ~~spinning~~ or stops spinning, ~~moving~~ respectively. As~~Once~~ the disk~~spindle~~ starts spinning~~motor begins to accelerate~~, the ~~read/write~~ heads is ~~are~~ dragged on~~to~~ the disks until the disks ~~accelerate to a~~ reaches a speed that creates sufficient air pressure for ~~at which~~ the heads ~~to will fly, or~~ separate~~,~~ from and fly over the disk ~~platter~~.

T~~To minimize the friction between the read/write head and the hard disk, the surface of t~~he disk can have ~~is usually textured to create~~ a "rough" texture ~~surface~~to minimize friction between the head and the disk in the landing zone. However, as disk drive ~~. As the~~ storage capacity ~~of hard disk drives~~ increases ~~every year~~, the flying height of the ~~read/write~~ heads decreases, and the disk is given a ~~. Thus, a hard disk surface must be very~~ smooth texture to avoid damaging ~~either~~ the heads ~~and/or the disk drive~~. The smooth texture dramatically increases ~~If, for example, the heads are parked onto the smooth surface of the disk,~~ the contact friction between the head and the disk in the landing zone~~increases dramatically~~. As a result, ~~an~~ increased spindle motor ~~in~~ current may be required to break the head loose from the disk ~~drive~~ to allow the disk ~~spindle~~ to rotate, or spin-up.

D~~This concern is relevant today as manufacturers of modern d~~isk drives have ~~are~~ increasingly ~~designing~~ smaller form factors, or disk sizes~~,~~ (2.5"~~"~~, 1.8"~~"~~ and 1"~~" so far~~). Small form factors are useful ~~, particularly~~ in battery-operated devices where i~~. An i~~ncreased spindle motor ~~in the~~ current to spin up the disk is

~~required to rotate the spindle is therefore~~ unnot desirable. SAdditionally, a ~~smaller~~ form factors reduces the disk surface area ~~and the total disk data area~~, which is reduced further by ~~if~~ a ~~separate~~ landing zone ~~is employed~~. SFinally, ~~smaller~~ form factors ~~disk drives~~ are also more susceptible to operational and non-operational shock~~, which could be more damaging~~ if the head and the disk are in contact. Thus, small form factors are penalized by a landing zone.

DTo overcome these constraints, disk drives have been designed with ~~manufacturers have implemented~~ a ramp to avoid a landing zone. The~~structure where the heads are lifted off the disk and are parked onto a separate ramp. In a ramp structure, the read/write heads do not fall to the surface of the disk when the disk's motor stops. Rather, the~~ heads is ~~are~~ lifted off ~~from the surface of~~ the disk ~~while the drive is still spinning~~ and unloaded ~~are parked~~ on the ~~to special~~ ramp while the disk is spinning, and then s~~. After the read/write heads have ascended the ramp,~~ the disks decelerates and stops spinning. When ~~the~~ power is reapplied to the spindle motor, ~~the process is reversed. T~~the disks spins up~~,~~ and once the disks has~~ve~~ sufficient ~~accelerated to a~~ speed for ~~such that~~ the head to~~s~~ fly ~~without contacting the disk surface~~, the heads is loaded from ~~are moved off~~ the ramps and positioned over ~~onto the surface of~~ the disk ~~platters~~.

During ~~a~~ ramp load/unload ~~procedure~~, the head velocity ~~of the read/write head~~ is accurately controlled to avoid damaging the head~~,~~ or the disk at a~~the~~ contact point ~~of contact, thereby compromising the disk drive reliability and quality~~. As the VCM~~actuator coil~~ moves through its magnetic poles, it generates a back electromotive field (EMF~~emf~~) voltage~~, ("V_{bemf}")~~, which is proportional to its speed. Th~~us,~~ e back EMF voltage also V_{bemf} ~~is an~~ indicates ~~or of the actuator velocity and therefore may be accurately measured to provide feedback of~~ the head velocity. The back EMF V_{bemf} voltage (Vbemf) can ~~may~~ be calculated based on the total voltage across the VCM (Vvcm) and the IR drop across the VCM (Ivcm *x* Rvcm) as follows:

$$Vbemf = Vvcm - (Ivcm \times Rvcm) \quad (1)$$

Thus, the back EMF voltage is measured by removing the VCM IR drop from the VCM voltage~~by first determining the overall voltage across the VCM coil. The total voltage across the VCM coil is: V_{bemf} + I_{vem}*R_{vem}. To measure the V_{bemf}, therefore, the term I_{vem}*R_{vem}, which represents the VCM "IR" drop, is removed from the equation, thereby isolating the V_{bemf} voltage~~.

There back EMF voltage can be measured by ~~are two methods by which the V_{bemf} voltage may be isolated and measured. First,~~ a pPulse wWidth mModulation (PWM) technique or ~~may be used. Second,~~ an IR cancellation technique ~~may be employed~~. In the ~~Pulse Width Modulation ("PWM")~~ technique, the VCM is turned off periodically, forcing the VCM current ~~in the VCM coil, I_{vem}, to go~~ to zero. Since ~~Thus,~~ the "IR" drop across the VCM is ~~coil equals~~ zero, ~~and~~ the back EMF V_{bemf} voltage is ~~may be~~ readily measured. In the IR cancellation technique, the back EMF V_{bemf} voltage is determined by measuring the gain of~~in~~ a servo loop. Since ~~Unlike the PWM technique, the current to~~ the VCM current is not periodically turned off ~~in the IR cancellation technique. Rather~~, ~~some~~ calibrations ~~may be required to~~ cancel the IR drop ~~component~~ from the VCM voltage. The ~~Such~~ calibrations may need to be repeated because temperature and voltage deviations ~~may~~ cause the gain of the servo loop to change frequently over time.

~~Of the two V_{bemf} measurement techniques discussed above, the PWM technique is easier to implement.~~ The PWM technique requires less hardware and fewer calibrations than the IR cancellation technique. However, ~~the load/unload process of the VCM in~~ the PWM technique may generate ~~be~~ audible noise during ramp load/unload~~and therefore inappropriate for applications in which audible noise is not desirable~~. The IR cancellation technique, however, ~~may itself not be appropriate for certain applications, as it is more sophisticated than the PWM technique and~~ requires ~~a~~ robust calibration ~~technique~~ with more ~~associated~~ hardware. ~~Further, an~~ increased voltage ~~in the~~ resolution ~~of the voltage measurements~~ may require a hardware ~~design~~ change to increase

~~because the resolution and accuracy of the measurements is a function of~~ the number of bits of the analog-to-digital ~~A/D~~ converter.

Disk drives have been ~~In the prior art, hardware had to be specifically~~ designed for either the PWM or IR cancellation techniques. If both techniques were needed ~~for a particular application~~, two distinct sets of hardware had to be implemented, thereby ~~possibly~~ increasing ~~the overall~~ cost ~~of the system~~. Further, ~~during the implementation of the measurement techniques, the~~ a ~~decision as to which~~ technique ~~would be employed~~ needed to be selected ~~made~~ before ~~prior to~~ any voltage measurements, thereby greatly reducing ~~the system~~ flexibility.

There is, therefore, ~~For the reasons stated above and for other reasons presented in greater detail in the detailed description of the present specification, there is~~ a need for a disk drive with ~~desire for a system that allows for the~~ accurate control of the ~~a disk read/write~~ head during ~~a~~ ramp load/unload ~~procedure~~. T~~In particular, t~~here is also a need for a disk drive that measures the back EMF voltage with ~~system that may employ~~ either the ~~a~~ PWM technique or the ~~an~~ IR cancellation ~~calibration~~ technique ~~to measure the back emf voltage~~ without ~~the need for~~ hardwiring a specific measurement technique or making multiple ~~system~~ calibrations prior to operation of the disk drive.

SUMMARY OF THE INVENTION

To achieve these and other advantages and in accordance with ~~the purposes of~~ the present invention, as embodied and broadly described, a method and apparatus for controlling the velocity of a ~~read/write disk~~ head during a ramp load/unload are disclosed.

A disk drive controls head velocity during ramp load/unload by measuring voltages across a VCM and a sense resistor in series with the VCM, calculating a

back EMF voltage using the VCM and sense resistor voltages, and adjusting the head velocity using the back EMF voltage.

An ~~According to an~~ embodiment ~~of the present invention, a method~~ includes amplifying the VCM and sense resistor voltages, multiplexing the amplified voltages, digitizing the multiplexed voltages and calculating the back EMF voltage in discrete-time based on the digitized voltages.

Another embodiment includes selecting between the PWM and IR cancellation techniques and calculating the back EMF voltage using the selected technique without two distinct sets of hardware.

Another embodiment includes calculating a calibration constant by comparing reference voltages across the VCM and the sense resistor while no current is applied to the VCM with voltages across the VCM and the sense resistor while current is applied to the VCM.

Another embodiment includes calculating a control variable in the discrete time domain using a proportional-integral control technique that compares a target head velocity to an actual head velocity and adjusting the head velocity based on the control variable. ~~for accurately measuring the V_{bemf} voltage using either of two different techniques; PWM and IR cancellation, and a means for making real-time adjustments to the velocity of the voice coil motor (VCM) is disclosed. The method includes measuring, amplifying, and transporting to a microprocessor the voltages across a voice coil motor (V_{motor}) and a sense resistor (V_{Rsense}). The method further includes calculating the V_{bemf} voltage of the VCM and making real-time adjustments to the VCM velocity.~~

~~According to another embodiment of the present invention, an apparatus to control the velocity of a transducer head during a ramp load/unload is disclosed. The control circuitry includes a driver circuit that powers the VCM, a multiplexer, an analog-to-digital converter (ADC), and a microprocessor. The microprocessor typically calculates the VCM velocity based on a measured V_{bemf} voltage.~~

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention are more fully described in the following drawings and accompanying text in which like reference numbers represent corresponding elements throughout:

FIG. 1 illustrates a ~~cross-section of a hard~~ disk drive ~~assembly~~;

FIG. 2 illustrates ~~a block diagram of the art~~ ramp load/unload ~~procedure~~;

FIG. 3 illustrates a ~~schematic of the~~ ramp load/unload control circuit ~~in accordance with a preferred embodiment of the present invention~~;

FIG. 4 ~~illustrate~~s a flowchart of a ~~microprocessor~~ calibration algorithm ~~in accordance with the present invention~~; and

FIG. 5 ~~illustrate~~s a flowchart of a load/unload algorithm ~~in accordance with the invention~~; and

FIG. 6 ~~illustrate~~s a flowchart of a velocity compensation algorithm ~~in accordance with the present invention~~.

DETAILED DESCRIPTION

FIG. 1 illustrates a conventional ~~depicts a prior art hard~~ disk drive 100 that ~~. The prior art hard disk drive 100~~ includes a ~~n actuator 110 having a~~ voice coil motor (VCM) 105, a disk~~s~~ 11~~2~~0~~, or platters~~, a cover 11~~5~~3~~0~~, an actuator arm 12~~4~~0, a spindle 12~~5~~0~~,~~ a DC power input 130, a read/write head~~s~~ 13~~5~~6~~0~~, a base casting 14~~7~~0, an I/O connector 145, a printed circuit board 150, a frame/bracket 155, a connector 160, a printed circuit cable 165 and a shock mount 170 ~~and sliders 180~~.

The ~~A hard disk drive 100 uses round flat~~ disk~~s~~ 11~~2~~0~~, or platters, that~~ is ~~are~~ coated on both sides with ~~a special~~ media ~~material~~ that ~~designed to~~ store~~s~~ information. The disk~~s~~ 11~~2~~0 is ~~are~~ mounted ~~and stacked~~ on~~to~~ the cylindrical spindle 12~~5~~0~~,~~ that, during operation, rotates the disk~~s~~ 11~~2~~0 at ~~a~~ high speed. The ~~Electromagnetic read/write~~ head~~s~~ 13~~5~~6~~0~~ is positioned over and ~~are mounted onto the sliders 180 and are used to record or~~ read~~s~~ ~~information to or~~ from and writes

to the disks 1120. The head 135 is embedded in a ~~The~~ sliders ~~180 are~~ mounted ~~onto~~ the actuator arms 1240. The VCM 105 and the actuator arm 120 form an actuator assembly that ~~are connected mechanically into a single assembly and positioned over the surface of the disk 120. The sliders 180 and the actuator arms 140~~ moves the ~~read/write~~ heads 13560 relative to the disk 110 as needed for read/write operations. The ~~hard~~ disk drive 100 is enclosed by the ~~a~~ cover 11530 and ~~a~~ the base casting 1470.

FIG. 2 illustrates ~~A~~ ramp load/unload in the disk ~~hard~~ drive 1200 ~~is illustrated in FIG. 2~~. The disk~~hard~~ drive 1200 includes a ramp 175, and the actuator arm 120 includes a lift tab 180. ~~210, a détente (rest) position 220, an actuator 110, an actuator arm 140, a disk 120, a slider 180, a read/write head 160, and a read/write position 240.~~ During read/write operations, the ~~read/write~~ heads 135160 ~~flies~~ over the ~~surface of the~~ disk 1120, at ~~a~~the read/write position 185240, ~~on as a result of~~ an air cushion caused by the rotation of the disks 1120. During ~~the~~ ramp unload, the VCM 105 ~~actuator 110~~ moves the ~~slider 180 and read/write~~ head 13560 from the disk 110 onto the ~~special~~ ramp 175210 while the disk 1120 is still spinning.

~~The read/write head 160 comes to rest at the détente position 220, which is used by the hard disk drive 200 as a landing zone on the hard drive 200.~~ After the ~~read/write~~ head 13560 comes to rest at a~~onto the~~ park ~~détente~~ position 19220, the ~~hard~~ disk drive 1200 stops the rotation of the disk 1120. Similarly, during ~~the~~ ramp load, the ~~hard~~ disk drive 1200 spins up ~~increases the rotation of~~ the disk 1120, and w~~.~~ ~~When~~ the disk 1120 ~~is~~ spins~~ning~~ at sufficient ~~a~~ velocity for ~~where~~ the ~~read/write~~ head 13560 to ~~can~~ fly above the disk 1120 ~~without making contact~~, the VCM ~~actuator~~ 10510 moves the ~~slider 180 and read/write~~ head 13560 from ~~off~~ the ~~special~~ ramp 175 ~~210~~ to ~~and onto~~ the disk 1120.

FIG. 3 illustrates ~~In order to control the velocity of the slider and the read/write head 160 up and down the ramp 210, one embodiment of the present invention uses~~ a ramp load/unload control circuit~~ry~~ 300. The control circuit~~ry~~ 300 includes a driver ~~circuit~~ 30510, a first operational amplifier 310, a second

operational amplifier 315, ~~that powers the VCM,~~ a multiplexer 32~~7~~0, an analog-to-digital converter (ADC) 325~~80,~~ and a microprocessor 33~~9~~0.

The VCM 105 has an internal resistance (Rvcm) 105A, a back EMF voltage (Vbemf) 105B and a total voltage (Vvcm). The VCM 105 is connected in series with a sense resistor 195 with a sense resistance (Rsense).

The driver 305 has a first output that is connected to the VCM 105 and a positive input of the first operational amplifier 310, and a second output that is connected to the sense resistor 195 and a negative input of the second operational amplifier 315. The VCM 105 is connected to the sense resistor 195, a negative input of the first operational amplifier 310 and a positive input of the second operational amplifier 315 at a node.

The driver 305 powers the VCM 105 by sending a current through the VCM 105 and the sense resistor 195. The first operational amplifier 310 receives and amplifies the total voltage across the VCM 105 (Vvcm). The second operational amplifier 315 receives and amplifies the voltage across the sense resistor 195 (Vrsense). The multiplexer 320 selects between the amplified VCM voltage from the first operational amplifier 310 at a first voltage path and the amplified sense resistor voltage from the second operational amplifier 315 at a second voltage path in response to a sample signal from the microprocessor 330. The ADC 325 coverts the multiplexed voltage selected by the multiplexer 320 from analog to digital format, and sends the digital signal along a serial port to the microprocessor 330.

~~T~~The microprocessor 33~~9~~0 calculates the back EMF voltage based on the VCM voltage and the sense resistor voltage, as amplified by the operational amplifiers 310 and 315, multiplexed by the multiplexer 320 and digitized by the ADC 325. The microprocessor 330 also ~~typically~~ calculates the VCM velocity based on the back EMF voltage, and sends a control signal to the driver 105 in a feedback loop to accurately control the head velocity.

The microprocessor 330 calculates the back EMF voltage by selecting between ~~a measured V_{bemf} voltage 340. There are two methods by which the back~~

~~emf voltage may be isolated and measured. First,~~ the PWM technique and the ~~Pulse Width Modulation may be used. Second, the~~ IR cancellation technique ~~may be employed~~. As a result, the disk drive 100 calculates the back EMF voltage using a selected one of the PWM technique and the IR cancellation technique without implementing two distinct sets of hardware.

~~In the Pulse Width Modulation ("PWM") technique, the VCM is turned off periodically, forcing the current in the VCM coil, I_{vcm}, to go to zero. Thus, the "IR" drop across the VCM coil equals zero and the bemf voltage, V_{bemf}, is readily measured. Unlike the PWM technique, the current to the VCM is not periodically turned off in the IR cancellation technique. Rather, some calibrations may be required to cancel the IR component from the VCM voltage. Such calibrations may need to be repeated because temperature and voltage deviations may cause the gain of the servo loop to change frequently over time. After it calculates the V_{bemf} voltage, the microprocessor 390 performs a control loop compensation before controlling the input to the driver circuitry 310. The output of a driver circuit 310 is connected to both a resistance of the voice coil motor, R_{vcm}, 320 and the positive input of a first operational amplifier 350.~~

~~When the read/write heads 160 are moved across the magnetic disk, the back emf voltage, V_{bemf} 340, opposes the motion of the heads 160. As the velocity of actuator arm 140 increases, the magnitude of V_{bemf} increases. To measure this voltage, an external sense resistor, Rsense 330 may be placed in series with V_{bemf} 340 and R_{vcm}, 320. Rsense 330 may then be connected to the negative input of the first operational amplifier 350 and to the positive input of a second operational amplifier 360. The other side of Rsense 330 may be connected to the negative input of the second operational amplifier 360 and to an output of the driver circuit 310.~~

~~The output of the first operational amplifier 350 and the output of the second operational amplifier 360 are coupled to a multiplexer 370. The operational amplifiers 350 and 360 output signals are referenced to a Reference voltage, Vref 357. An analog to digital converter (ADC) 380 converts the~~

~~multiplexed analog signals into a digital format before they are received by microprocessor 390. The microprocessor 390 calculates the VCM velocity, as described below in Figure 4, does the desired control loop compensation, and sends the appropriate control signal to the input of the driver circuit 310.~~

~~When the disk drive is initialized at power-up, the driver circuit 310 is off and the current to the VCM, $I_{vcm,}$ is zero. At this point, the transducer heads are stationary, and the back emf voltage, V_{bemf} 340, is 0. The microprocessor 390 receives a voltage level from the first operational amplifier 350, Vvcm 353, which is equal to Vref 357, and designates the voltage as Vref1. The microprocessor 390 then receives a voltage level from the second operational amplifier 360, which is equal to Vref 357, and designates it as Vref2. To determine the exact offset in each path, Vref is measured through the paths of Vvcm 353 and the sense resistor, V_{Rsense}.~~

~~The microprocessor 390 then determines the output level in both paths of Vvcm 353 and V_{Rsense} 355 for the ADC 380 voltage corresponding to no current flowing in the VCM coils.~~ The microprocessor 3390 calibrates the control circuit~~ry~~ 300 using the~~the~~ calibration algorithm 400 described below. The~~is method of~~ calibration algorithm 400 calculates a~~the~~ gain calibration constant ~~gain coefficient,~~ (Kcal)~~,~~ using the following IR cancellation technique:

~~Kcal may be defined as:~~

$$Kcal = \frac{i \times Rvcm \times Kvcm}{i \times Rsense \times Ksense}$$ (~~Equation~~ 2~~1~~)

~~if~~ $Kvcm = 1$ ~~and~~ $Ksense = 1$ then

$$Kcal = \frac{i \times Rvcm}{i \times Rsense}$$

(~~Equation~~ 3~~2~~)

At start-up, a small VCM current is applied towards the outer crash stop making the back EMF voltage zeroV_{bemf} ~~340 = 0~~:

$$i \times Rvcm = Vvcm - Vref1$$

(Equation 3)

$$i \times Rsense = Vrsense - Vref2$$

(Equation 4)

Therefore, the following relationship is established:

$$i \times Rvcm = Kcal \times (i \times Rsense)$$

(Equation 5)

Substitution yields the following equality:

$$-(Vvcm - Vref1) = Kcal \times (Vrsense - Vref2)$$

(Equation 6)

The microprocessor 390 calibrates the control circuit 300 by determining the calibration constant (Kcal) as follows:

$$Kcal = \frac{Vvcm - Vref1}{Vrsense - Vref2}$$

(Equation 7)

After calibrating the control circuit 300, the microprocessor 390 monitors the back EMF voltage V_{bemf} at sample times to determine whether to increase or decrease the current controlling the head velocity.

Figure 4 illustrates a flow chart of a calibration algorithm 400 that the control circuit 300 implements to determine a gain calibration constant (Kcal) at power-up of the disk drive 100. At step 405, the calibration algorithm 400 starts. At step 410, the driver 305 turns off the current to the VCM 105. At step 415, the microprocessor 390 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense) to provide a first reference voltage (Vref1) and a second reference voltage (Vref2) respectively. At step 420, the driver 305 applies a small current to the VCM 105 to move the heads 135 in the unload direction (towards a crash stop, away from the disk 110). At step 425, the

multiplexer 320 selects the VCM voltage (Vvcm), and at step 430, the multiplexer 320 selects the sense resistor voltage (Vrsense). At step 435, ~~before the microprocessor 390 selects and reads the VCM voltage, Vvcm 353, step 440. The microprocessor 390 selects and reads the sense voltage, V_{Rsense} 355, step 450. In step 460,~~ the microprocessor 3390 calculates the calibration constant~~, Kcal,~~ (Kcal) according to ~~a~~equation (8).~~:~~

~~$$Kcal = \frac{Vvcm - Vref1}{Vrsense - Vref2}$$ (Equation 8)~~ At step 440, t~~T~~he calibration algorithm 400 ends ~~at step 470~~.

~~_____~~ Figure 5 ~~illustrate~~s a flow chart of a load/unload algorithm 500 that the control circuit~~ry~~ 300 implements to control the velocity of the ~~read/write~~ head~~s~~ 13560 during ramp~~a~~ load/unload ~~procedure, as illustrated in Figure 2~~. At step 505, the load/unload ~~The~~ algorithm starts ~~at step 505~~. At step 510, t~~T~~he microprocessor 3390 determines whether the ~~read/write~~ heads 13560 is ~~are~~ being loaded from or unloaded onto~~from~~ the ramp 175~~, step 510~~. If the head~~s~~ 135 is ~~are~~ being loaded from the ramp 175, then at step 515 the microprocessor 330 sets the voltage corresponding to the~~a~~ target velocity of the ~~read/write~~ heads 13560 (~~as~~ Vload–t~~Load_T~~arget)~~, step 515~~. At step 520, t~~T~~he microprocessor 3390 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense)~~then receives the Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380, step 520~~. At ~~In~~ step 525, the microprocessor 3390 calculates the back EMF~~emf~~ voltage (~~,~~ Vbemf~~bemf 340~~)~~,~~ as follows:

$$Vbemf = (Vvcm - Vref1) - Kcal \times (Vrsense - Vref2)$$

(~~Equation~~ 9)

At~~In~~ step 530, the microprocessor 3390 ~~uses the~~ calculate~~sd value for V_{bemf} 340 to determine~~ a velocity error (Verr) as follows:

$$Verr = Vloadtarget - Vbemf$$

(~~Equation~~ 10)

At~~In~~ step 535, the microprocessor 3390 performs the~~a~~ velocity compensation algorithm 600 ~~as~~ described below ~~in Figure 6~~ to ~~make~~ adjust~~ments~~

~~to~~ the ~~read/write head~~ velocity of the head 135~~60~~. ~~The velocity compensation algorithm adjusts the transducer head velocity by comparing the voltage corresponding to the load target velocity with the voltage corresponding to the actual velocity of the transducer heads, as determined from V_{bemf} 340.~~

~~At~~In step 540, the microprocessor 339~~0~~ determines whether the ~~read/write~~ heads 135~~60~~ is ~~have~~ loaded on ~~to~~ the disk 112~~0~~. If the loading procedure is not complete, then at step 545 the microprocessor 339~~0~~ waits for the next sampling period and then the process returns to step 520~~one sample duration in step 547 before transferring control to step 520~~ to measure ~~receive~~ the next VCM voltage (Vvcm) and sense resistor voltage (Vrsense)~~Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380~~. If the loading procedure ~~of the read/write head onto the disk~~ is complete, then at step 550 the head 135 is locked into tracking mode and at step 595 ~~the heads are locked into tracking mode, in step 545, before~~ the load/unload algorithm 500 ends~~concludes at step 590~~.

~~-~~Returning to ~~In~~ step 515~~0~~, if the microprocessor 339~~0~~ determines that the ~~read/write~~ heads 135~~60~~ is~~are~~ being unloaded onto the ramp 175~~210~~, then at step 555 the microprocessor 339~~0~~ sets the voltage corresponding to ~~assigns~~ the target velocity of the head 135 (Vunloadtarget)~~as V_Unload_Target~~. At step 560, the microprocessor 330 measures the VCM voltage (Vvcm) and the sense resistor voltage (Vrsense). ~~The microprocessor 390 then receives the Vvcm 353 and V_{Rsense} 355 voltages from the ADC 380 in step 555.~~ At step 565~~In step 560~~, the microprocessor 339~~0~~ ~~may~~ calculates the back EMF voltage (Vbemf)~~bemf 340~~ according to equation (9).~~:~~

~~$Vbemf = (Vvcm - Vref1) - Kcal \times (Vrsense - Vref2)$ (Equation 9)~~

~~At~~ Using the calculated value for V_{bemf} 340, in step 570~~65~~ the microprocessor 339~~0~~ calculates ~~may determine~~ the velocity error (~~,~~Verr)~~,~~ as follows:

Verr = Vu~~_~~Unloadt~~_~~Target – Vbemf~~–~~ V_{bemf}

(~~Equation~~ 11)

At step 575, tThe microprocessor 3390 ~~then~~ performs the velocity compensation algorithm 600 ~~as~~ described below ~~in Figure 6~~ to ~~make any necessary~~ adjust~~ments~~ ~~to~~ the velocity of the ~~read/write~~ head 1356~~0 velocity, step 570. The velocity compensation algorithm adjusts the velocity of the transducer heads by comparing the voltage corresponding to the load target velocity with the voltage corresponding to the actual velocity of the transducer heads, as determined from V_{bemf} 340.~~

~~——~~ At step 580, tThe microprocessor 3390 ~~next~~ determines whether the ~~unloading of the read/write~~ head is unloaded from the disk 110~~has successfully completed, step 575~~. If the unloading procedure is~~has~~ not complete~~d~~, then at step 585 the microprocessor 3390 waits for the next ~~one~~ sampling~~ing~~ period and then the process returns to step 560 to measure the next VCM voltage (Vvcm) and sense resistor voltage (Vrsense)~~before transferring control to step 555 to receive the Vvcm 353 and V_{Rsense} 355 voltage measurements, step 580~~. ~~If~~ the unloading procedure i~~has~~ complete~~d~~, then at step 590 the VCM 105 is disabled and at ~~,~~step 5985 t~~. The~~ load/unload algorithm 500 ends ~~at step 590~~.

Figure 6 i~~llustrate~~s a flow chart of a ~~the~~ velocity compensation algorithm 600 that ~~initiated by~~ the microprocessor 3390 initiates to correct the velocity of the ~~read/write~~ heads 13560. At step 605, tThe velocity compensation algorithm 600 begins ~~at step 610~~. At step 610, tThe microprocessor 330 ~~first~~ determines the ~~value of the~~ velocity error (~~,~~Verr(n))~~,~~ for the current sample ~~period, step 620. This may be done,~~ as previously described in steps 530 or 5706~~5~~ of the load/unload algorithm 500. At step 615

~~——~~ ~~Next~~, the microprocessor 330 determines ~~the value of~~ a discrete control variable (c~~,~~ ~~C~~ontrol(n))~~,~~ that will be used by the driver ~~circuit~~ 3105 to ~~make~~ adjust~~ments to~~ the head velocity. Although ~~there are~~ several methods of velocity compensation ~~that~~ are well known in the art and may be employed in the present invention, the preferred embodiment ~~of the present invention~~ employs a~~the~~ p~~P~~roportional-i~~I~~ntegral control technique, where~~in~~ Kp is a proportional constant and Ki an integral constant. Both Kp and Ki are selected according to the

desired frequency and transient responses for the velocity control loop. The proportional-integral control technique calculates the discrete control variable ~~basic equation,~~ in the continuous time domain~~, for the velocity compensation algorithm 600 may be represented~~ as follows:

$$Output\_command = \left(Kp + \frac{Ki}{S}\right) \times Verr \qquad \text{(Equation 12)}$$

~~Although a continuous time domain illustration is shown, the preferred embodiment of the present invention employs a microprocessor 390 that digitally processes the control signals. The above output control equation should therefore be implemented in the discrete time domain. In step 630, therefore, t~~The microprocessor 3390 calculates the ~~value for the~~ discrete control variable (c~~,~~ ~~C~~ontrol(n)) in the discrete time domain~~,~~ using the proportional-integral control technique as follows:

$$Control(n) = Control(n-1) + Ki \times (T - Kp) \times Verr(n-1) + Kp \times (Verr(n)), \qquad \text{(Equation (13)}$$

where (n) denotes the current sample and (n—1) denotes the previous sample. The discrete control variable corrects the head velocity by comparing the voltage corresponding to the target velocity with the voltage corresponding to the actual velocity of the head 135 as determined by the back EMF voltage.

At step 620, t~~T~~he microprocessor 3390 ~~then~~ sends the discrete control variable ~~value for Control(n)~~ to the driver ~~circuit~~ 3105, and the driver 305 ~~where~~ adjust~~ments~~ ~~to~~ the head velocity based on the discrete control variable~~will be initiated, step 640~~. At step 625, ~~Using the current values for Control(n) and Verr(n),~~ the microprocessor 3390 sets the discrete control variable and the velocity error of the current sample (control(n) and Verr(n)) to the previous sample (control(n–1) and Verr(n–1)) for use by the next sample~~value of Control(n-1) and Verr(n-1) equal to the current values of Control(n) and Verr(n), so that these values may be used for velocity control during the next sample time, step 650~~. At step 630, the microprocessor 330 determines whether ~~If~~ the velocity

compensationg algorithm 600 continues. If so, then the process returns to step 610 for the next sample, otherwise at step 635 tcontrol is transferred to step 620 wherein the microprocessor determines the value of the velocity error, Verr(n), for the current sample period. The velocity compensation- algorithm 600 endsconcludes at step 660.

EXAMPLE

The present invention is illustrated by the following By way of example, the following calculations represent an illustrative implementation of the present invention. TTypical values for the VCM resistance and the sense resistors are as followsmay be:

Rvcm 320 = 17.1 Ω

Rsense 330 = 1 Ω

TSimilarly, the gains of the first operational amplifier 3150 (Kvcm), and the second operational amplifier 31560, (Krsense) are as followsmay be:

Kvcm = 5

Krsense = 4

The ADC 325 preferred embodiment of the invention utilizes a 12-bits ADC converter 380 with a full-scale voltage of 5 volts and has the following . Thus, the resolution of the preferred ADC converter 380 may be:

$$ADC\_resolution = \frac{ADC\_FS\_voltage}{2^{ADC\_bits} - 1} = \frac{5}{2^{12} - 1} = 1.221.10^{-3} \text{—V/count}$$

(Equation 14)

The driver 305 provides a reference voltage of 2.5 volts to the sense resistor 195 and the second operational amplifier 315 , Vref 357, when V_{bemf} 340 = 0, may be 2.5 voltswhen the back EMF voltage is zero. The first and second reference voltages Because different offset voltages may exist for the paths of Vvcm and V_{Rsense}, the reference voltage through each path may not be identical to

~~Vref 357. If~~ (Vref1 and Vref2) are as follows~~defined as the reference voltages at the ADC 380 for each respective path, these voltages may be~~:

$Vref1 = 2.520$ volts~~; and~~

$Vref2 = 2.510$ volts~~.~~

Th~~us, the~~ ADC ~~380~~ counts corresponding to the first and second reference voltages at the first and second voltage ~~for each~~ paths are as follows~~would be~~:

$$ADC\_Vref1\_count = \frac{Vref1.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2064$$

$$ADC\_Vref2\_count = \frac{Vref2.2^{ADC\_bits}}{ADC\_FS\_voltage} = 2056$$

The VCM voltage (Vvcm) when ~~Setting~~ the VCM current (Ivcm)~~vcm~~ is~~to~~ 10 mA is as follows~~may then yield a value for Vvcm 353 of~~:

$Vvcm = Vref1 + Ivcm \times Rvcm \times$

~~$Vvcm.353 = Vref1 + Ivcm \times Rvcm.320 \times Kvcm$~~ $Kvcm$

$= -2.52$ v + 10 mA x* 17.1 Ω x* 5

$= 3.375$ volts

The ADC ~~converter 380~~ count corresponding to ~~this~~ Vvcm ~~voltage 353~~ is as follows:

$$ADC\_Vvcm\_count = Integer\left(\frac{Vvcm.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref1\_count\right)$$

~~(Equation 15)~~

$= -(3.375$ v x* 4096) / 5v – 2064

$= -701$

The ~~Similarly, the ADC converter 380 count corresponding to the~~ V_{Rsense} ~~355 may be calculated by first determining the value of~~ Vrsense$_{Rsense}$ ~~355~~ is as follows:

$Vrsense = Vref2 + Ivcm \times Rsense \times Ksense$ ~~(Equation 16)~~

$= 2.51 + 10$ mA x* 1 Ω x* 4

$= -2.55$ volts

This ~~value of V_{Rsense} 355 corresponde~~s to the ~~following~~ ADC ~~380~~ count corresponding to Vrsense is as follows:

$$ADC\_Vrsense\_count = Integer\left(\frac{Vrsense.2^{ADC\_bits}}{ADC\_FS\_voltage} - ADC\_Vref2\_count\right)$$

~~(Equation 17)~~

= -(2.55 v x* 4096) / 5v – 2056

= 33

Finally, the ~~value for the~~ calibration constant (~~gain,~~ Kcal) ~~, for the preferred embodiment~~ is ~~determined~~ as follows:

$$Kcal = \frac{ADC\_Vvcm\_count}{ADC\_Vrsense\_count} \quad \text{~~(Equation 18)~~}$$

= —700 / 33

= –21.21

T~~It should be understood that t~~he number of bits in the ADC 3258~~0~~ may be increased if greater accuracy or resolution is desired, or ~~the number of bits in the ADC 380 may be~~ reduced to decrease computational burden.

It will be apparent to those skilled in the art that various modifications and variations can be made to the embodiments described above ~~hard disk drive ramp load/unload methodology~~ without departing from the spirit or the scope of the invention. Thus, it is intended that the present invention covers ~~the~~ modifications and variations ~~of this invention provided~~ that ~~they~~ come within ~~the scope of the~~ any claims and their equivalents.

ABSTRACT

A disk drive controls head velocity during ramp load/unload by measuring voltages across a VCM and a sense resistor in series with the VCM, calculating a back EMF voltage using the VCM and sense resistor voltages, and adjusting the head velocity using the back EMF voltage. An embodiment includes amplifying the VCM and sense resistor voltages, multiplexing the amplified voltages, digitizing the multiplexed voltages and calculating the back EMF voltage in discrete-time based on the digitized voltages. Another embodiment includes selecting between PWM and IR cancellation techniques and calculating the back EMF voltage using the selected technique. ~~The present invention provides a hard drive assembly and a related method for measuring the velocity of a transducer head during a ramp load/unload. To achieve these and other advantages and in accordance with the purposes of the present invention, as embodied and broadly described, a method and apparatus for controlling the velocity of a read/write disk head during a ramp load/unload are disclosed. The method includes measuring, amplifying, and transporting to a microprocessor the voltages across a voice coil motor (V_{motor}) and a sense resistor (V_{Rsense}). The method further includes calculating the V_{bemf} voltage of the VCM and making real-time adjustments to the VCM velocity. The apparatus used to control the velocity of a read/write disk head during a ramp load/unload includes a driver circuit that powers the VCM, a multiplexer, an analog-to-digital converter (ADC), and a microprocessor. The microprocessor typically calculates the VCM velocity based on a measured V_{bemf} voltage.~~